# EXHIBIT 7

# FILED UNDER SEAL

UNITED STATES PATENT AND TRADEMARK OFFICE

———————————

BEFORE THE PATENT TRIAL AND APPEAL BOARD

———————————

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

———————————

IPR2022-00237
Patent 10,268,608 B2

———————————

Before JON M. JURGOVAN, NABEEL U. KHAN, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

KHAN, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
*35 U.S.C. § 314, 37 C.F.R. § 42.4*

| Electronic Patent Application Fee Transmittal | |
|---|---|
| **Application Number:** | 15820076 |
| **Filing Date:** | 21-Nov-2017 |
| **Title of Invention:** | MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Filer:** | Gary Scott Williams/Edith Fuentes |
| **Attorney Docket Number:** | 129980-5049US |

Filed as Large Entity

Filing Fees for   Utility under 35 USC 111(a)

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | |
| **Extension-of-Time:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Miscellaneous:** | | | | |
| RCE- 1ST REQUEST | 1801 | 1 | 1300 | 1300 |
| **Total in USD ($)** | | | | **1300** |

164

# Electronic Acknowledgement Receipt

| | |
|---|---|
| **EFS ID:** | 33912832 |
| **Application Number:** | 15820076 |
| **International Application Number:** | |
| **Confirmation Number:** | 8866 |
| **Title of Invention:** | MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Customer Number:** | 79141 |
| **Filer:** | Gary Scott Williams/Edith Fuentes |
| **Filer Authorized By:** | Gary Scott Williams |
| **Attorney Docket Number:** | 129980-5049US |
| **Receipt Date:** | 03-OCT-2018 |
| **Filing Date:** | 21-NOV-2017 |
| **Time Stamp:** | 20:36:27 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | yes |
| Payment Type | DA |
| Payment was successfully received in RAM | $1300 |
| RAM confirmation Number | 100418INTEFSW00006576500310 |
| Deposit Account | |
| Authorized User | |
| The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: | |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Request for Continued Examination (RCE) | 129980-5049US_RCE.pdf | 93171<br><br>e02dxd71e63d8d63c4d5c6159adee13c8a1295f6a | no | 1 |

**Warnings:**

This is not a USPTO supplied RCE SB30 form.

**Information:**

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 2 | | 129980-5049US_IDS-1st-IDS-w-RCE.pdf | 603273<br><br>9fd0a719277629e24e8f9ad3822e991370d92b8a | yes | 22 |

| Multipart Description/PDF files in .zip description | | |
|---|---|---|
| Document Description | Start | End |
| Transmittal Letter | 1 | 4 |
| Information Disclosure Statement (IDS) Form (SB08) | 5 | 22 |

**Warnings:**

**Information:**

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 3 | | 129980-5049US_IDS-2nd-IDS-w-RCE.pdf | 400555<br><br>7c8cdf5593c9017879f554a5c502e9fcda1a13a | yes | 31 |

| Multipart Description/PDF files in .zip description | | |
|---|---|---|
| Document Description | Start | End |
| Transmittal Letter | 1 | 2 |
| Information Disclosure Statement (IDS) Form (SB08) | 3 | 31 |

**Warnings:**

**Information:**

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 4 | Fee Worksheet (SB06) | fee-info.pdf | 30627<br><br>512eaea02576ca0faf9d03cdcc67364e1acf0105a | no | 2 |

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| Warnings: | |
|---|---|
| Information: | |
| **Total Files Size (in bytes):** | 1127626 |

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

# NOTICE OF ALLOWANCE AND FEE(S) DUE

7914    7552    07/03/2018

Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

| EXAMINER |
|---|
| SUN, MICHAEL |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2184 | |

DATE MAILED: 07/03/2018

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 15/820,076 | 11/21/2017 | Hyun Lee | 129980-5049US | 8866 |

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $1000 | $0 | $0 | $1000 | 10/03/2018 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.   THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT.  SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED.  THIS STATUTORY PERIOD CANNOT BE EXTENDED.  SEE 35 U.S.C. 151.  THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION.  IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

## HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.**

PTOL-85 (Rev. 02/11)

**PART B - FEE(S) TRANSMITTAL**

Complete and send this form, together with applicable fee(s), to: **Mail**

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141    7583    07/03/2018
Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

|  |
|---|
| (Depositor's name) |
| (Signature) |
| (Date) |

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 15/820,076 | 11/21/2017 | Hyun Lee | 129980-5049US | 8866 |

TITLE OF INVENTION: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $1000 | $0 | $0 | $1000 | 10/03/2018 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| SUN, MICHAEL | 2184 | 710-310000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address for Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,    1

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.    2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE    (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) :    ❑ Individual    ❑ Corporation or other private group entity    ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____    Date _____

Typed or printed name _____    Registration No. _____

Page 2 of 3

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PTOL-85 Part B (10-13) Approved for use through 10/31/2013.    OMB 0651-0033    U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 15/820,076 | 11/21/2017 | Hyun Lee | 129980-5049US | 8866 |

79141    7590    07/03/2018
Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

| EXAMINER |
|---|
| SUN, MICHAEL |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2184 | |

DATE MAILED: 07/03/2018

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

## OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

## Privacy Act Statement

**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

| **Notice of Allowability** | Application No. 15/820.076 | Applicant(s) LEE ET AL. | |
|---|---|---|---|
| | Examiner MICHAEL SUN | Art Unit 2184 | AIA (First Inventor to File) Status No |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Applicant's Amendment filed 5/24/2018*.

    ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____ .

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-12*. As a result of the allowed claim(s). you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp  or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    Certified copies:

    a) ☐ All    b) ☐ Some    *c) ☐ None of the:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

        3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

    * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.

    ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

    Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)

2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____

3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

4. ☐ Interview Summary (PTO-413). Paper No./Mail Date _____ .

5. ☐ Examiner's Amendment/Comment

6. ☒ Examiner's Statement of Reasons for Allowance

7. ☐ Other _____ .

/MICHAEL SUN/
Primary Examiner, Art Unit 2184

Application/Control Number: 15/820,076                                        Page 2

Art Unit: 2184

The present application is being examined under the pre-AIA first to invent provisions.

## DETAILED ACTION

### Status of the Application

This Office Action is in response to Applicant's Amendment filed 5/24/2018.

Claims 1-12 are pending for this examination.

Claim 1 was amended.

Claims 2-12 were added.

### Terminal Disclaimer

The terminal disclaimer filed on 5/24/2018 disclaiming the terminal portion of any patent

granted on this application which would extend beyond the expiration date of US Patent No.

9,128,632; US Patent No. 9,563,587; and US Patent No. 9,824,035 has been reviewed and is

accepted. The terminal disclaimer has been recorded.

### Allowable Subject Matter

Claims 1-12 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art teaches memory module systems arranged into respective groups of memory

devices, memory module systems with buffered memory modules, and memory module systems

that implement delays for transmitting signals to the memory devices of each module, however,

the prior art does not fairly teach or suggest, individually or in combination, a memory module

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Art Unit: 2184

system with a plurality of buffers mounted in positions corresponding to the respective sets of

data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines

and a set of memory devices and including logic that responds to control signals by enabling the

data paths corresponding to memory operations between the data / strobe signal lines and the

memory devices, wherein the logic is configured to obtain timing information based on signals

received by the buffers during a second memory operation prior to the first memory operation

and to control timing of the data and strobe signals on the data paths in accordance with the

obtained timing information as claimed. These limitations find support in Applicant's

Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the

above recited combination.


Any comments considered necessary by applicant must be submitted no later than the

payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for

Allowance."


## Contact Information

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to MICHAEL SUN whose telephone number is (571)270-1724.

The examiner can normally be reached on Monday-Thursday 6:45am-4:45pm.

Examiner interviews are available via telephone, in-person, and video conferencing using

a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is

Application/Control Number: 15/820,076                                                Page 4

Art Unit: 2184

encouraged to use the USPTO Automated Interview Request (AIR) at

http://www.uspto.gov/interviewpractice.

   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be

obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


/MICHAEL SUN/

Primary Examiner, Art Unit 2184

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|---|---|---|---|---|---|---|
| **Notice of References Cited** | | | Application/Control No.<br>15/820,076 | | Applicant(s)/Patent Under Reexamination<br>LEE ET AL. | |
| | | | Examiner<br>MICHAEL SUN | | Art Unit<br>2184 | Page 1 of 1 |

## U.S. PATENT DOCUMENTS

| * | | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Name | CPC Classification | US Classification |
|---|---|---|---|---|---|---|
| * | A | US-2014/0029370 A1 | 01-2014 | KOSHIZUKA: Atsuo | G11C7/1051 | 365/233.13 |
| | B | US- | | | | |
| | C | US- | | | | |
| | D | US- | | | | |
| | E | US- | | | | |
| | F | US- | | | | |
| | G | US- | | | | |
| | H | US- | | | | |
| | I | US- | | | | |
| | J | US- | | | | |
| | K | US- | | | | |
| | L | US- | | | | |
| | M | US- | | | | |

## FOREIGN PATENT DOCUMENTS

| * | | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Country | Name | CPC Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
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| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
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## NON-PATENT DOCUMENTS

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | |
| | V | |
| | W | |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U S Patent and Trademark Office
PTO-892 (Rev. 01-2001)                    **Notice of References Cited**                    Part of Paper No 20180623

| **Issue Classification** | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 15820076 | LEE ET AL. |
| | Examiner | Art Unit |
| | MICHAEL SUN | 2184 |

### CPC

| Symbol | | | | | Type | Version |
|---|---|---|---|---|---|---|
| G06F | | 13 | | 1673 | F | 2013-01-01 |
| G06F | | 3 | | 0659 | I | 2013-01-01 |
| G11C | | 16 | | 00 | I | 2013-01-01 |
| G11C | | 5 | | 04 | I | 2013-01-01 |
| G11C | | 7 | | 1006 | I | 2013-01-01 |
| G11C | | 7 | | 1066 | I | 2013-01-01 |
| G11C | | 7 | | 109 | A | 2013-01-01 |
| G11C | | 7 | | 1093 | I | 2013-01-01 |
| G11C | | 8 | | 12 | A | 2013-01-01 |
| G06F | | 1 | | 10 | I | 2013-01-01 |
| G06F | | 3 | | 0613 | I | 2013-01-01 |
| G06F | | 3 | | 0647 | I | 2013-01-01 |
| G06F | | 3 | | 0683 | I | 2013-01-01 |
| G06F | | 13 | | 28 | I | 2013-01-01 |
| G06F | | 13 | | 4027 | I | 2013-01-01 |
| G06F | | 3 | | 0656 | I | 2013-01-01 |
| G06F | | 13 | | 1642 | I | 2013-01-01 |
| G11C | | 8 | | 18 | I | 2013-01-01 |
| G11C | | 7 | | 20 | A | 2013-01-01 |
| G11C | | 29 | | 023 | I | 2013-01-01 |
| G11C | | 29 | | 028 | I | 2013-01-01 |
| H05K | | 999 | | 99 | I | 2013-01-01 |
| G11C | | 2029 | | 0407 | A | 2013-01-01 |

### CPC Combination Sets

| Symbol | | | Type | Set | Ranking | Version |
|---|---|---|---|---|---|---|
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| NONE | | Total Claims Allowed: |
|---|---|---|
| (Assistant Examiner) | (Date) | 12 |
| /MICHAEL SUN/<br>Primary Examiner.Art Unit 2184 | 06/23/2018 | O.G. Print Claim(s)    O.G. Print Figure |
| (Primary Examiner) | (Date) | 1      1 |

U.S. Patent and Trademark Office      Part of Paper No. 20180623

| *Issue Classification* | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| ‖‖‖‖‖‖‖‖‖‖‖ | 15820076 | LEE ET AL. |
| | **Examiner** | **Art Unit** |
| | MICHAEL SUN | 2184 |

| US ORIGINAL CLASSIFICATION | | INTERNATIONAL CLASSIFICATION | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **CLASS** | **SUBCLASS** | **CLAIMED** | | | | | **NON-CLAIMED** | |
| 710 | 5 | G | 0 | 6 | F | 3 00 (2006 01 01) | | |
| **CROSS REFERENCE(S)** | | G | 0 | 6 | F | 12 00 (2006 01 01) | | |
| | | G | 0 | 6 | F | 13 00 (2006 01 01) | | |

| CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) | | | | |
|---|---|---|---|---|---|
| 710 | 6 | 7 | | | |
| 711 | ' | 2 | 3 | 4 | '54 |
| 711 | '55 | | | | |
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| NONE | | **Total Claims Allowed:** | |
|---|---|---|---|
| (Assistant Examiner) | (Date) | 12 | |
| /MICHAEL SUN/ Primary Examiner, Art Unit 2184 | 06/23/2018 | O.G. Print Claim(s) | O.G. Print Figure |
| (Primary Examiner) | (Date) | 1 | 1 |

U S Patent and Trademark Office                                                              Part of Paper No  20180623

| *Issue Classification* | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 15820076 | LEE ET AL. |
| | **Examiner** | **Art Unit** |
| | MICHAEL SUN | 2184 |

| ☐ Claims renumbered in the same order as presented by applicant | ☐ CPA | ☒ T.D. | ☐ R.1.47 |
|---|---|---|---|

| Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original |
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| 1 | 1 | | | | | | | | | | | | | | |
| 2 | 2 | | | | | | | | | | | | | | |
| 3 | 3 | | | | | | | | | | | | | | |
| 4 | 4 | | | | | | | | | | | | | | |
| 5 | 5 | | | | | | | | | | | | | | |
| 6 | 6 | | | | | | | | | | | | | | |
| 7 | 7 | | | | | | | | | | | | | | |
| 8 | 8 | | | | | | | | | | | | | | |
| 9 | 9 | | | | | | | | | | | | | | |
| 10 | 10 | | | | | | | | | | | | | | |
| 11 | 11 | | | | | | | | | | | | | | |
| 12 | 12 | | | | | | | | | | | | | | |
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| NONE | | Total Claims Allowed: |
|---|---|---|
| | | 12 |
| (Assistant Examiner) | (Date) | |
| /MICHAEL SUN/ Primary Examiner.Art Unit 2184 | 06/23/2018 | O.G. Print Claim(s) · O.G. Print Figure |
| (Primary Examiner) | (Date) | 1 · 1 |

U.S. Patent and Trademark Office

Part of Paper No. 20180623

**EAST Search History**

**EAST Search History (Prior Art)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| S260 | 5100 | memory module and timing signal | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:30 |
| S261 | 2127 | S260 and memory controller | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:30 |
| S262 | 213 | S261 and operating speed | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:30 |
| S263 | 76 | S262 AND (( (G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC. ) OR (710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS.) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:30 |
| S264 | 76 | S263 and buffer | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:30 |
| S265 | 76 | S264 and ((data or strobe) near2 signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:30 |
| S266 | 76 | S265 and (read or write) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:30 |
| S267 | 46 | S266 and memory bus | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:30 |
| S268 | 9 | S267 and command signal | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:30 |
| S269 | 4852 | (lee, hyun).in. | US-PGPUB; USPAT; USOCR; EPO; DERWENT; | ADJ | ON | 2018/06/23 06:30 |

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| S270 | 113 | (bhakta, jayesh).in. | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:30 |
|---|---|---|---|---|---|---|
| S271 | 603648 | buffer and memory and (data or strobe) and (read or write) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:31 |
| S272 | 60216 | S271 and ((determin$5 or calculat$3) with (time interval or delay)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:31 |
| S273 | 139 | S271 and ((determin$5 or calculat$3) with (time interval or delay) with (first signal) with (second signal)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:31 |
| S274 | 58 | S273 and (transmi$5 with (time interval or delay)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:31 |
| S275 | 793 | (determining or calculating) with (time interval or delay) with (first signal) with (second signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:32 |
| S276 | 1 | S275 and memory controller and buffer and memory bus | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:32 |
| S277 | 6213 | memory module and buffer and memory device and memory controller and control signal and command | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:33 |
| S278 | 988 | S277 and system clock | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:33 |
| S279 | 41 | S278 and (write with (different near4 time)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:33 |
| S280 | 9 | S279 and (align$4 with read) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:33 |
| S281 | 180115 | (deriving or timing or calculating) with (delay or latency) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; | ADJ | ON | 2018/06/23 06:35 |

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| | | | | | | |
|---|---|---|---|---|---|---|
| S282 | 2169 | S281 and read and write and strobe and memory module and controller | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:35 |
| S283 | 1781 | S282 and buffer | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:35 |
| S284 | 1751 | S283 and ((data or strobe) near4 signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:35 |
| S285 | 354 | S284 and (timing with transmission) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:35 |
| S286 | 72 | S285 and (timing with transmission with read) with write | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:35 |
| S287 | 8353 | memory module and buffer and tim$3 and (control signal or address signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2018/06/23 06:36 |
| S288 | 1737 | S287 and time interval | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:36 |
| S289 | 1302 | S288 and delay | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:36 |
| S290 | 372 | S289 and (strobe signal and data signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:36 |
| S291 | 10 | S290 and (time interval with (first signal and second signal)) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:36 |
| S292 | 10 | S291 and memory controller | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | ON | 2018/06/23 06:36 |
| S293 | 7 | S292 and time transmission | US-PGPUB; USPAT; USOCR; EPO; DERWENT; | ADJ | ON | 2018/06/23 06:36 |

| | | | IBM_TDB | | | |
|---|---|---|---|---|---|---|
| S294 | 440 | memory module and buffer and (control signal and address signal and data signal and strobe signal) | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2018/06/23 06:37 |
| S295 | 323 | S294 and delay | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2018/06/23 06:37 |
| S296 | 160 | S295 and time interval | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2018/06/23 06:37 |
| S297 | 141 | S296 and memory controller | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2018/06/23 06:37 |
| S298 | 51 | S297 and tim$3 transmission | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2018/06/23 06:37 |
| S299 | 14 | S298 and first signal and second signal | US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB | ADJ | OFF | 2018/06/23 06:37 |

**EAST Search History (Interference)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| S300 | 4730 | ((710/5 OR 710/6 OR 710/7 OR 711/1 OR 711/2 OR 711/3 OR 711/4 OR 711/154 OR 711/155).CCLS. OR (G06F1/12 OR G06F13/1689 OR G06F12/0246 OR G06F13/1694).CPC. ) and (memory).clm. and (buffer).clm. | US-PGPUB; USPAT | ADJ | ON | 2018/06/23 13:54 |
| S301 | 417 | S300 and (delay or time interval).clm. | US-PGPUB; USPAT | ADJ | ON | 2018/06/23 13:54 |
| S302 | 275 | S301 and (read or write).clm. | US-PGPUB; USPAT | ADJ | ON | 2018/06/23 13:54 |
| S303 | 3 | S302 and (time transmitting or time transmission).clm. | US-PGPUB; USPAT | ADJ | ON | 2018/06/23 13:54 |

6/23/2018 2:02:47 PM
C:\ Users\ msun\ Documents\ EAST\ Workspaces\ 15820076.wsp

| *Search Notes* | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 15820076 | LEE ET AL. |
| ‖‖‖‖‖‖‖‖‖‖‖‖‖ | **Examiner** | **Art Unit** |
| | MICHAEL SUN | 2184 |

## CPC- SEARCHED

| Symbol | Date | Examiner |
|---|---|---|
| limited search of G06F 1/12 | 6/23/2018 | MS |
| limited search of G06F 13/1689 | 6/23/2018 | MS |
| limited search of G06F 12/0246 | 6/23/2018 | MS |
| limited search of G06F 13/1694 | 6/23/2018 | MS |

## CPC COMBINATION SETS - SEARCHED

| Symbol | Date | Examiner |
|---|---|---|
| | | |

## US CLASSIFICATION SEARCHED

| Class | Subclass | Date | Examiner |
|---|---|---|---|
| | | | |

\* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

## SEARCH NOTES

| Search Notes | Date | Examiner |
|---|---|---|
| Updated EAST Search - see attached | 6/23/2018 | MS |
| Inventor Search - see attached EAST Search | 6/23/2018 | MS |
| limited EAST Search of class/subclasses 710/5, 6, and 7 | 6/23/2018 | MS |
| limited EAST Search of class/subclasses 711/1, 2, 3, 4, 154, and 155 | 6/23/2018 | MS |
| Google Scholar Search - search terms used: (memory module and buffering); (memory and buffer and tristate buffer); (memory and tristate buffer and delay) | 6/23/2018 | MS |

## INTERFERENCE SEARCH

| | /MICHAEL SUN/<br>Primary Examiner, Art Unit 2184 |
|---|---|
| | |

| US Class/ CPC Symbol | US Subclass / CPC Group | Date | Examiner |
|---|---|---|---|
| 710 | limited search of subclasses 5, 6, and 7 | 6/23/2018 | MS |
| 711 | limited search of subclasses 1, 2, 3, 4, 154, and 155 | 6/23/2018 | MS |
| G06F | limited search of 1/12, 13/1689, 12/0246, and 13/1694 | 6/23/2018 | MS |

| | /MICHAEL SUN/ Primary Examiner, Art Unit 2184 |
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

## BIB DATA SHEET

**CONFIRMATION NO. 8866**

| SERIAL NUMBER | FILING or 371(c) DATE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 15/820,076 | 11/21/2017 <br> **RULE** | 710 | 2184 | 129980-5049US |

**APPLICANTS**
Netlist, Inc., Irvine, CA;

**INVENTORS**
Hyun Lee, Ladera Ranch, CA;
Jayesh R. Bhakta, Cerritos, CA;

**\*\* CONTINUING DATA \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\***
This application is a CON of 15/426,064 02/07/2017 PAT 9824035
    which is a CON of 14/846,993 09/07/2015 PAT 9563587
    which is a CON of 13/952,599 07/27/2013 PAT 9128632
    which claims benefit of 61/676,883 07/27/2012

**\*\* FOREIGN APPLICATIONS \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\***

**\*\* IF REQUIRED, FOREIGN FILING LICENSE GRANTED \*\***
12/20/2017

| | | | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|---|
| Foreign Priority claimed ☐ Yes ☑ No <br> 35 USC 119(a-d) conditions met ☐ Yes ☑ No <br> Verified and Acknowledged   MICHAEL SUN <br> Examiner's Signature | ☐ Met after Allowance <br> Initials | | CA | 26 | 4  12 | 1 |

**ADDRESS**

Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304
UNITED STATES

**TITLE**

MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

| FILING FEE RECEIVED <br> 1600 | FEES: Authority has been given in Paper <br> No._____ to charge/credit DEPOSIT ACCOUNT <br> No._____ for following: | ☐ All Fees |
|---|---|---|
| | | ☐ 1.16 Fees (Filing) |
| | | ☐ 1.17 Fees (Processing Ext. of time) |
| | | ☐ 1.18 Fees (Issue) |
| | | ☐ Other _____ |
| | | ☐ Credit |

BIB (Rev. 05-07)

| | PTO/SB/26 |
|---|---|
| Doc Code: DIST.E.FILE<br>Document Description: Electronic Terminal Disclaimer - Filed | U.S. Patent and Trademark Office<br>Department of Commerce |

| Electronic Petition Request | **TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT** |
|---|---|
| Application Number | 15820076 |
| Filing Date | 21-Nov-2017 |
| First Named Inventor | Hyun Lee |
| Attorney Docket Number | 129980-5049US |
| Title of Invention | MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS |

☒   Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒   This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

| Owner | Percent Interest |
|---|---|
| NETLIST, INC. | 100% |

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

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9563587

9824035

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

○ Small Entity

○ Micro Entity

◉ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

   Registration Number  51167

○ A sole inventor

○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

○ A joint inventor; all of whom are signing this request

| Signature | / Jamie J. Zheng / |
|-----------|--------------------|
| Name | Jamie J. Zheng |

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

188

## Electronic Patent Application Fee Transmittal

| | |
|---|---|
| **Application Number:** | 15820076 |
| **Filing Date:** | 21-Nov-2017 |
| **Title of Invention:** | MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Filer:** | Jamie Jie Zheng |
| **Attorney Docket Number:** | 129980-5049US |

Filed as Large Entity

Filing Fees for  Utility under 35 USC 111(a)

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| STATUTORY OR TERMINAL DISCLAIMER | 1814 | 1 | 160 | 160 |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| Extension-of-Time: | | | | |
| Miscellaneous: | | | | |
| **Total in USD ($)** | | | | 160 |

190

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.:  15820076

Filing Date:     21-Nov-2017

Applicant/Patent under Reexamination:    Lee

Electronic Terminal Disclaimer filed on    May 24, 2018

☒    APPROVED

    **This patent is subject to a terminal disclaimer**

☐    DISAPPROVED

Approved/Disapproved by:  Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

# Electronic Acknowledgement Receipt

| | |
|---|---|
| **EFS ID:** | 32709570 |
| **Application Number:** | 15820076 |
| **International Application Number:** | |
| **Confirmation Number:** | 8866 |
| **Title of Invention:** | MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Customer Number:** | 79141 |
| **Filer:** | Jamie Jie Zheng |
| **Filer Authorized By:** | |
| **Attorney Docket Number:** | 129980-5049US |
| **Receipt Date:** | 24-MAY-2018 |
| **Filing Date:** | 21-NOV-2017 |
| **Time Stamp:** | 16:49:23 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | yes |
| Payment Type | DA |
| Payment was successfully received in RAM | $ 160 |
| RAM confirmation Number | 052518INTEFSW00006558500310 |
| Deposit Account | |
| Authorized User | |
| The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: | |

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Terminal Disclaimer-Filed (Electronic) | eTerminal-Disclaimer.pdf | 33939 <br> d7670117605cd606c6l6cf9d6ec09ccd674 23036 | no | 2 |

**Warnings:**

**Information:**

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 2 | Fee Worksheet (SB06) | fee-info.pdf | 30555 <br> 31c0fc79cd0115c45cd04512fd6f3a0cd42 60509 | no | 2 |

**Warnings:**

**Information:**

| | Total Files Size (in bytes): | 64494 |
|---|---|---|

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**New Applications Under 35 U.S.C. 111**
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
**National Stage of an International Application under 35 U.S.C. 371**
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
**New International Application Filed with the USPTO as a Receiving Office**
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed May 24, 2018

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Application of: | Hyun Lee et al. | Confirmation No.: | 8866 |
| Serial No.: | 15/820,076 | Art Unit: | 2184 |
| Filed: | November 21, 2017 | Examiner: | Sun, Michael |
| For: | *MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS* | Attorney Docket No.: | 129980-5049-US |
| | | Date: May 24, 2018 | |

## RESPONSE TO OFFICE ACTION & INTERVIEW SUMMARY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

The enclosed Amendment is in response to the Office Action dated January 25, 2018 for the above identified patent application.

Petition for Extension of Time under 37 CFR 1.136. It is respectfully requested that the time for responding to the Office Action dated January 25, 2018 be extended for a period of one month from April 25, 2018 to May 25, 2018.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US).

McKesson Statement starts on page 2 of this paper.

Amendment to the Claims starts on Page 3 of this paper.

Remarks start on Page 6 of this paper.

## McKesson Statement

In view of *McKesson Information Solutions v. Bridge Medical* (Fed. Cir. 2007), Applicant wishes to inform the Examiner that the prosecution history of the following US Patent Application(s) may contain information relevant to the pending application:

(1) U.S. Application Serial No. 13/970,606, filed August 20, 2013. This application issued as U.S. Patent No. 9,606,907.

(2) U.S. Application Serial No. 15,470,856, filed March 27, 2017.

The Examiner is encouraged to review the art made of record, office actions and the notice(s) of allowance, if any, in the above-mentioned applications, all of which are available on PAIR.

| Electronic Patent Application Fee Transmittal | |
|---|---|
| **Application Number:** | 15820076 |
| **Filing Date:** | 21-Nov-2017 |
| **Title of Invention:** | MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Filer:** | Jamie Jie Zheng |
| **Attorney Docket Number:** | 129980-5049US |

Filed as Large Entity

Filing Fees for   Utility under 35 USC 111(a)

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Basic Filing:** | | | | |
| **Pages:** | | | | |
| **Claims:** | | | | |
| **Miscellaneous-Filing:** | | | | |
| **Petition:** | | | | |
| **Patent-Appeals-and-Interference:** | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | |
| **Extension-of-Time:** | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
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| Extension - 1 month with $0 paid | 1251 | 1 | 200 | 200 |
| **Miscellaneous:** | | | | |
| | | **Total in USD ($)** | | **200** |

197

# Electronic Acknowledgement Receipt

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|---|---|
| **EFS ID:** | 32717177 |
| **Application Number:** | 15820076 |
| **International Application Number:** | |
| **Confirmation Number:** | 8866 |
| **Title of Invention:** | MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS |
| **First Named Inventor/Applicant Name:** | Hyun Lee |
| **Customer Number:** | 79141 |
| **Filer:** | Jamie Jie Zheng |
| **Filer Authorized By:** | |
| **Attorney Docket Number:** | 129980-5049US |
| **Receipt Date:** | 24-MAY-2018 |
| **Filing Date:** | 21-NOV-2017 |
| **Time Stamp:** | 16:51:59 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

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|---|---|
| Submitted with Payment | yes |
| Payment Type | DA |
| Payment was successfully received in RAM | $200 |
| RAM confirmation Number | 052518INTEFSW00006893500310 |
| Deposit Account | |
| Authorized User | |
| The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: | |

198

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | | 129980_5049US_AMEND.pdf | 153831<br><br>d717c2f64d838950e3ueoa123v6e4os6de86217 | yes | 7 |

| | Multipart Description/PDF files in .zip description | | | | |
|---|---|---|---|---|---|
| | **Document Description** | | **Start** | **End** | |
| | Applicant Arguments/Remarks Made in an Amendment | | 6 | 7 | |
| | Claims | | 3 | 5 | |
| | Amendment/Req. Reconsideration-After Non-Final Reject | | 1 | 2 | |

**Warnings:**

**Information:**

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 2 | Fee Worksheet (SB06) | fee-info.pdf | 30970<br><br>8e609912a06ksark 18725u85759ex519 3c13 | no | 2 |

**Warnings:**

**Information:**

| | | |
|---|---|---|
| **Total Files Size (in bytes):** | | 184801 |

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

## *REMARKS*

This amendment responds to the office action mailed January 25, 2018. In the office action, the Examiner:

A. rejected claim 1 on the ground of nonstatutory obviousness-type double patenting.

## REMARKS CONCERNING CLAIMS

Claim 1 has been amended for minor issues.

Claims 2-12 have been added.

No new matter has been added.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 1-12.

## REMARKS CONCERNING DOUBLE PATENTING REJECTIONS

**A.    Rejection of claim 1 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632**

Applicant submits herewith a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d), which should overcome the nonstatutory obviousness-type double patenting rejection over claims 1-22 of US Patent No. 9,824,035; claims 1-20 of US Patent No. 9,563,587; and claims 1-20 of US Patent No. 9,128,632.

## CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the Examiner, Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In particular, Applicant's filing of the terminal disclaimer is for the sole purpose of expediting prosecution. It should not be understood as implying that Applicant agrees with the rejection of claim 1 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-7249, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date:    May 24, 2018          /Jamie J. Zheng/                              51167

Jamie J. Zheng                              (Reg. No.)
**MORGAN, LEWIS & BOCKIUS LLP**
1400 Page Mill Road
Palo Alto, CA 94304
Phone: (650) 843-7249

DB2/ 33351823.1

**Amendments to the Claims**

The following listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1.      (Currently Amended) A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective signal lines in the memory bus;

a module control device mounted on the module board and configured to receive command signals for memory operations ~~a first operation~~ via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the memory operations ~~first operation~~ in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock, wherein the data path corresponding to the each data signal line includes at least one ~~a~~ tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount

determined by the command processing circuit in response to at least one of the module control signals.

2.      (New) The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation, wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation, wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals, wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal through the data path is a signal associated with the second memory operation.

3.      (New) The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks, wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and wherein the second set of module command signals include chip select signals that select the at least one memory device in the respective set of memory devices from one of the plurality of ranks to perform the second memory operation.

4.      (New) The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

5.      (New) The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

6.      (New) The memory module of claim 1, wherein the each respective buffer circuit further includes a receiver circuit for each of the module control signals, the receiver circuit including a

metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal.

7.    (New) The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

8.    (New) The memory module of claim 6, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

9.    (New) The memory module of claim 1, wherein the each respective buffer circuit further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal, wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.

10.    (New) The memory module of claim 9, wherein the data paths include a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation, the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.

11.    (New) The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

12.    (New) The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

PTO SB 06 (09-11)
Approved for use through 1 31 2014 OMB 0651-0032
U.S. Patent and Trademark Office  U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

| PATENT APPLICATION FEE DETERMINATION RECORD<br>Substitute for Form PTO-875 | Application or Docket Number<br>15/820,076 | Filing Date<br>11/21/2017 | ☐ To be Mailed |
|---|---|---|---|

ENTITY:  ☒ LARGE  ☐ SMALL  ☐ MICRO

## APPLICATION AS FILED – PART I

| | (Column 1) | (Column 2) | | |
|---|---|---|---|---|
| FOR | NUMBER FILED | NUMBER EXTRA | RATE ($) | FEE ($) |
| ☐ BASIC FEE<br>(37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | |
| ☐ SEARCH FEE<br>(37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | |
| ☐ EXAMINATION FEE<br>(37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | |
| TOTAL CLAIMS<br>(37 CFR 1.16(i)) | minus 20 = | * | X $ = | |
| INDEPENDENT CLAIMS<br>(37 CFR 1.16(h)) | minus 3 = | * | X $ = | |
| ☐ APPLICATION SIZE FEE<br>(37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | |

## APPLICATION AS AMENDED – PART II

| | | (Column 1) | | (Column 2) | (Column 3) | | |
|---|---|---|---|---|---|---|---|
| AMENDMENT | 05/24/2018 | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) |
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| | Independent (37 CFR 1.16(h)) | * 1 | Minus | *** 3 | = 0 | x $460 = | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | |
| | | | | | | TOTAL ADD'L FEE | 0 |

| | | (Column 1) | | (Column 2) | (Column 3) | | |
|---|---|---|---|---|---|---|---|
| AMENDMENT | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE ($) | ADDITIONAL FEE ($) |
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| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | X $ = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | |
| | | | | | | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
VIOLA ROGERS

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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| APPLICATION NUMBER | FILING OR 371(C) DATE | FIRST NAMED APPLICANT | ATTY. DOCKET NO./TITLE |
|---|---|---|---|
| 15/820,076 | 11/21/2017 | Hyun Lee | N3044.10009US05 |

CONFIRMATION NO. 8866

**PUBLICATION NOTICE**

79141
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

*OC000000098581462*

Title:MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

**Publication No.**US-2018-0095908-A1
**Publication Date:**04/05/2018

## NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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page 1 of 1

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 15/820,076 | 11/21/2017 | Hyun Lee | N3044.10009US05 | 8866 |

| 75141          7590     01/25/2018 | | EXAMINER |
|---|---|---|
| Jamie J. Zheng, Ph.D Esq. | | SUN, MICHAEL |
| MASCHOFF BRENNAN | | |
| 1389 Center Drive | | |
| Suite 300 | ART UNIT | PAPER NUMBER |
| Park City, UT 84098 | 2184 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 01/25/2018 | ELECTRONIC |

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The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com
bisraelsen@mabr.com

208

| **Office Action Summary** | Application No. 15/820,076 | Applicant(s) LEE ET AL. |
|---|---|---|
| | Examiner MICHAEL SUN | Art Unit 2184 / AIA (First Inventor to File) Status No |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on _11/21/2017_.
  ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**.    2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims***

5)☒ Claim(s) _1_ is/are pending in the application.
  5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) _1_ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined <u>allowable</u>, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

**Application Papers**

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on _11/21/2017_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

  a)☐ All    b)☐ Some** c)☐ None of the:

  1.☐ Certified copies of the priority documents have been received.

  2.☐ Certified copies of the priority documents have been received in Application No. _____.

  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)

2)☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

4)☐ Other: _____.

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The present application is being examined under the pre-AIA first to invent provisions.

## DETAILED ACTION

### Status of the Application

This Office Action is in response to Applicant's Continuation filed on 11/21/2017.

Claim 1 is pending for this examination.

### Obvious-Type Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the

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scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination

under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP

§§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor

to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR

1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used.

Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the

form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or

PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely

online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-

processed and approved immediately upon submission. For more information about eTerminal

Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.


Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as

being unpatentable over claims 1-22 of copending Application No. 15/426,064, now US Patent

No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No.

9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No.

9,128,632. Although the conflicting claims are not identical, they are not patentably distinct

from each other because claim 1 of instant Application, respectively contains every element of

claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-

20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of

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copending Application No. 13/952,599, now US Patent No. 9,128,632, as listed below, and as

such anticipate the claims of the copending application:

| Claims | Instant Application | Claims | copending Application No. 13/952,599, now US Patent No. 9,128,632 |
|---|---|---|---|
| Independent claim 1 | A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:<br><br>a module board having edge connections for coupling to respective signal lines in the memory bus;<br><br>a module control device mounted on the module board and configured to receive command signals for a first operation via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and<br><br>memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the first operation in | Independent claim 1 | A memory module to operate in a memory system with a memory controller, the memory system operating according to a system clock, the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:<br><br>a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to each of the memory command signals;<br><br>memory devices organized in groups, each group including at least one memory device, the memory devices receiving the module command signals from the module control device and performing one or more memory operations in accordance with the module command signals; and<br><br>a plurality of buffer circuits to receive the module control signals, each respective buffer |

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| | response to the module command signals, the memory' devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and | | circuit corresponding to a respective group of memory devices and coupled between the respective group of memory devices and a respective set of the plurality of sets of data/strobe signal lines, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals; and |
|---|---|---|---|
| | a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and, a respective set of memory devices, and configured to receive the module control signals and the module clock, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock, wherein the data path corresponding to the each data signal line includes a tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module | | wherein the plurality of buffer circuits are distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines such that each module control signal arrives at the plurality of buffer circuits at different points in time, and<br><br>wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation. |

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|  | control signals. |  |  |
|---|---|---|---|
| Analysis | Examiner points out that the instant claim language is similar to the claim language of copending Application No. 13/952,599, now US Patent No. 9,128,632, and as such would be rendered obvious over the already allowed claim language of copending Application No. 13/952,599, now US Patent No. 9,128,632. |  |  |

Likewise, the dependent claims of the above cited independent claims carry similar

limitations to each other respectively.

| Claims | Instant Application | Claims | copending Application No. 15/426,064, now US Patent No. 9,824,035 |
|---|---|---|---|
| Independent claim 1 | A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:<br><br>a module board having edge connections for coupling to respective signal lines in the memory bus;<br><br>a module control device mounted on the module board and configured to receive command signals for a first operation via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module | Independent claim 1 | A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:<br><br>a module board having edge connections for coupling to respective data/strobe signal lines in the memory bus;<br><br>a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to produce module command signals and module control signals in response to the memory |

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| | control device being further configured to receive a system clock signal and output a module clock signal; and<br><br>memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the first operation in response to the module command signals, the memory' devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and<br><br>a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and, a respective set of memory devices, and configured to receive the module control signals and the module clock, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module | | command signals; and<br><br>memory devices mounted on the module board to perform a first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; and<br><br>a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit providing data paths between a respective set of the data/strobe signal lines and a respective set of the plurality of sets of memory' devices, the each respective buffer circuit including logic that responds to the module control signals by enabling a subset of the data paths for transmitting data and strobe signals corresponding to the first memory operation between the respective set of the data/strobe signal lines and the corresponding set of the plurality of sets of memory devices, wherein the logic is further configured to obtain timing information based on signals received by the each respective buffer circuit during a second memory operation prior to the first memory |

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| | | | |
|---|---|---|---|
| | clock, wherein the data path corresponding to the each data signal line includes a tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals. | | operation and to control timing of the data and strobe signals on the subset of the data paths in accordance with the timing information. |
| Analysis | Examiner points out that the instant claim language is similar to the claim language of copending Application No. 15/426,064, now US Patent No. 9,824,035, and as such would be rendered obvious over the already allowed claim language of copending Application No. 15/426,064, now US Patent No. 9,824,035. | | |

Likewise, the dependent claims of the above cited independent claims carry similar

limitations to each other respectively.

| Claims | **Instant Application** | Claims | **copending Application No. 14/846,993, now US Patent No. 9,563,587** |
|---|---|---|---|
| Independent claim 1 | A memory module operable to communicate with a memory controller via a memory bus. the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:<br><br>a module board having edge connections for coupling to respective signal lines in the memory bus; | Independent claim 1 | A memory module operable to communicate with a memory controller via a memory bus. the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:<br><br>a module board including edge connections for connecting to respective ones of the signal lines in the memory bus; |

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| | | | |
|---|---|---|---|
| | a module control device mounted on the module board and configured to receive command signals for a first operation via the set of control/address signal lines and to output module command signals and module control signals in response to the command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and<br><br>memory devices mounted on the module board and configured to receive the module command signals and the module clock, and to perform the first operation in response to the module command signals, the memory' devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and<br><br>a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and, a respective set of memory devices, and configured to receive the module control signals and the module clock, | | memory devices mounted on the module board, including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines;<br><br>buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit being coupled between a respective set of the data/strobe signal lines and a corresponding set of memory devices; and<br><br>a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to control the memory devices and the buffer circuits in response to the memory command signals;<br><br>wherein the each respective buffer circuit is configured to respond to one or more first control signals from the module control device by receiving write data/strobe signals from the respective set of data/strobe signal lines and transmitting the write data/strobe signals to the corresponding set of memory devices during a memory write operation; |

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| | | | |
|---|---|---|---|
| | the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock, wherein the data path corresponding to the each data signal line includes a tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals. | | wherein the each respective buffer circuit is further configured to respond to one or more second control signals from the module control device by receiving read data/strobe signals from the corresponding set of memory devices and transmitting the read data/strobe signals to the memory controller via the respective set of data/strobe signal lines during a memory read operation subsequent to the memory write operation; and<br><br>wherein the each respective buffer circuit is further configured to time the transmission of the read data/strobe signals during the read operation based on timing information derived from receiving the one or more first control signals and the write data/strobe signals during the write operation. |
| Analysis | Examiner points out that the instant claim language is similar to the claim language of copending Application No. 14/846,993, now US Patent No. 9,563,587, and as such would be rendered obvious over the already allowed claim language of copending Application No. 14/846,993, now US Patent No. 9,563,587. | | |

Likewise, the dependent claims of the above cited independent claims carry similar

limitations to each other respectively.

**<u>Allowable Subject Matter</u>**

Claim 1 is allowed.

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The following is an examiner's statement of reasons for allowance:

Prior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module, however, the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a plurality of buffers mounted in positions corresponding to the respective sets of data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines and a set of memory devices and including logic that responds to control signals by enabling the data paths corresponding to memory operations between the data / strobe signal lines and the memory devices, wherein the logic is configured to obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information as claimed. These limitations find support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

**Contact Information**

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Any inquiry concerning this communication or earlier communications from the

examiner should be directed to MICHAEL SUN whose telephone number is (571)270-1724.

The examiner can normally be reached on Monday-Thursday 6:45am-4:45pm.

Examiner interviews are available via telephone, in-person, and video conferencing using

a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is

encouraged to use the USPTO Automated Interview Request (AIR) at

http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be

obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


/MICHAEL SUN/

Primary Examiner, Art Unit 2184